

FIG. 1A
(PRIOR ART)

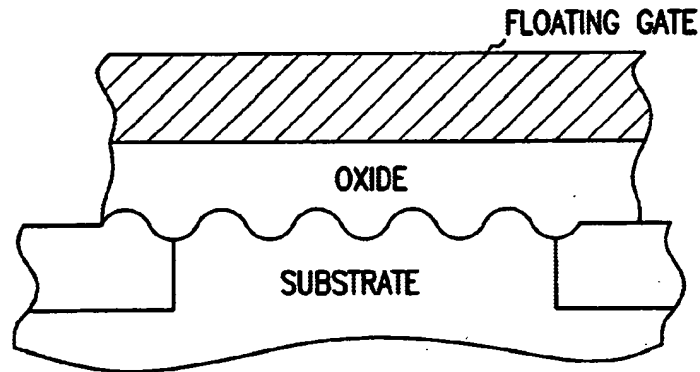


FIG. 1B
(PRIOR ART)



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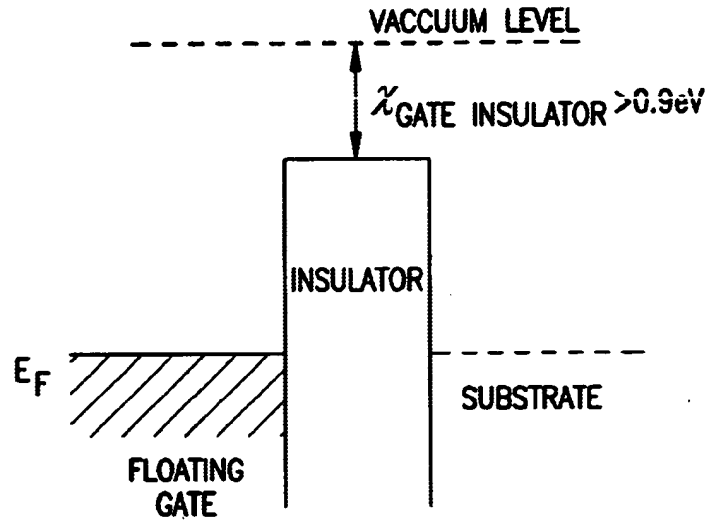


FIG. 1C
 (PRIOR ART)

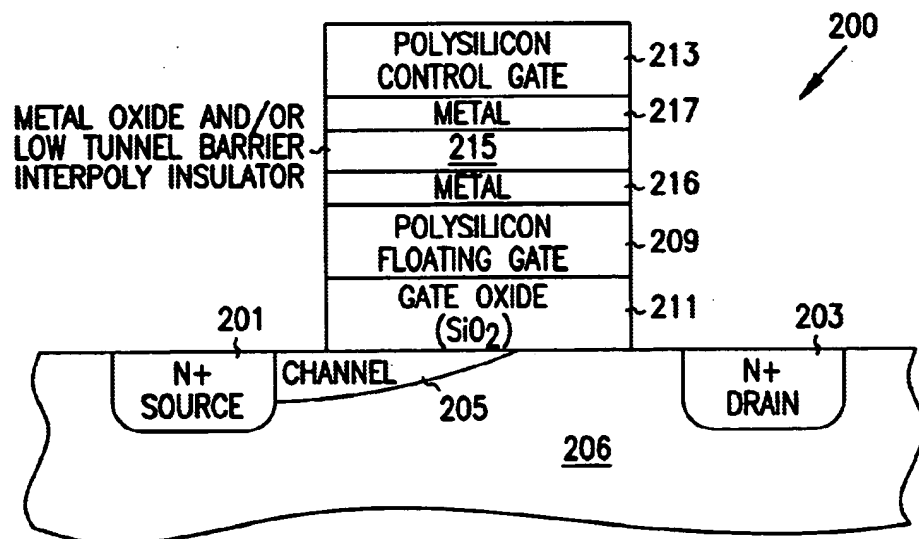


FIG. 2



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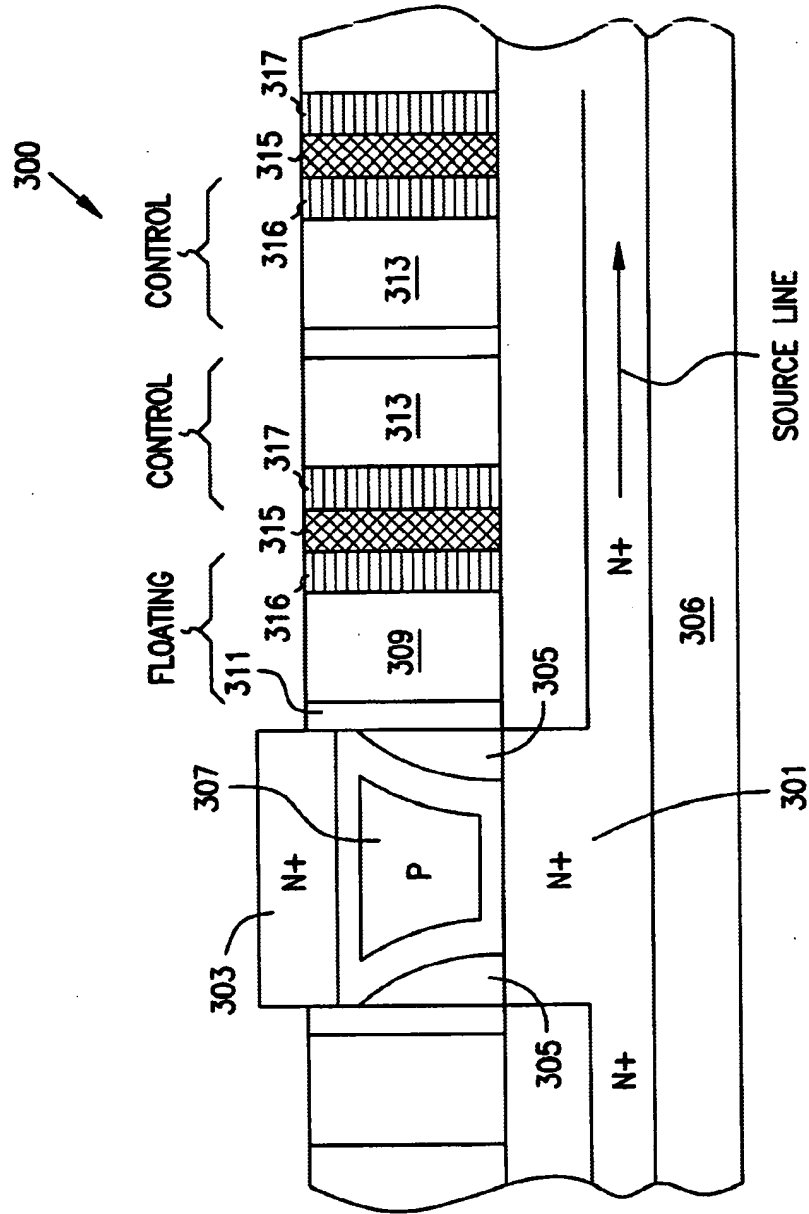


FIG. 3



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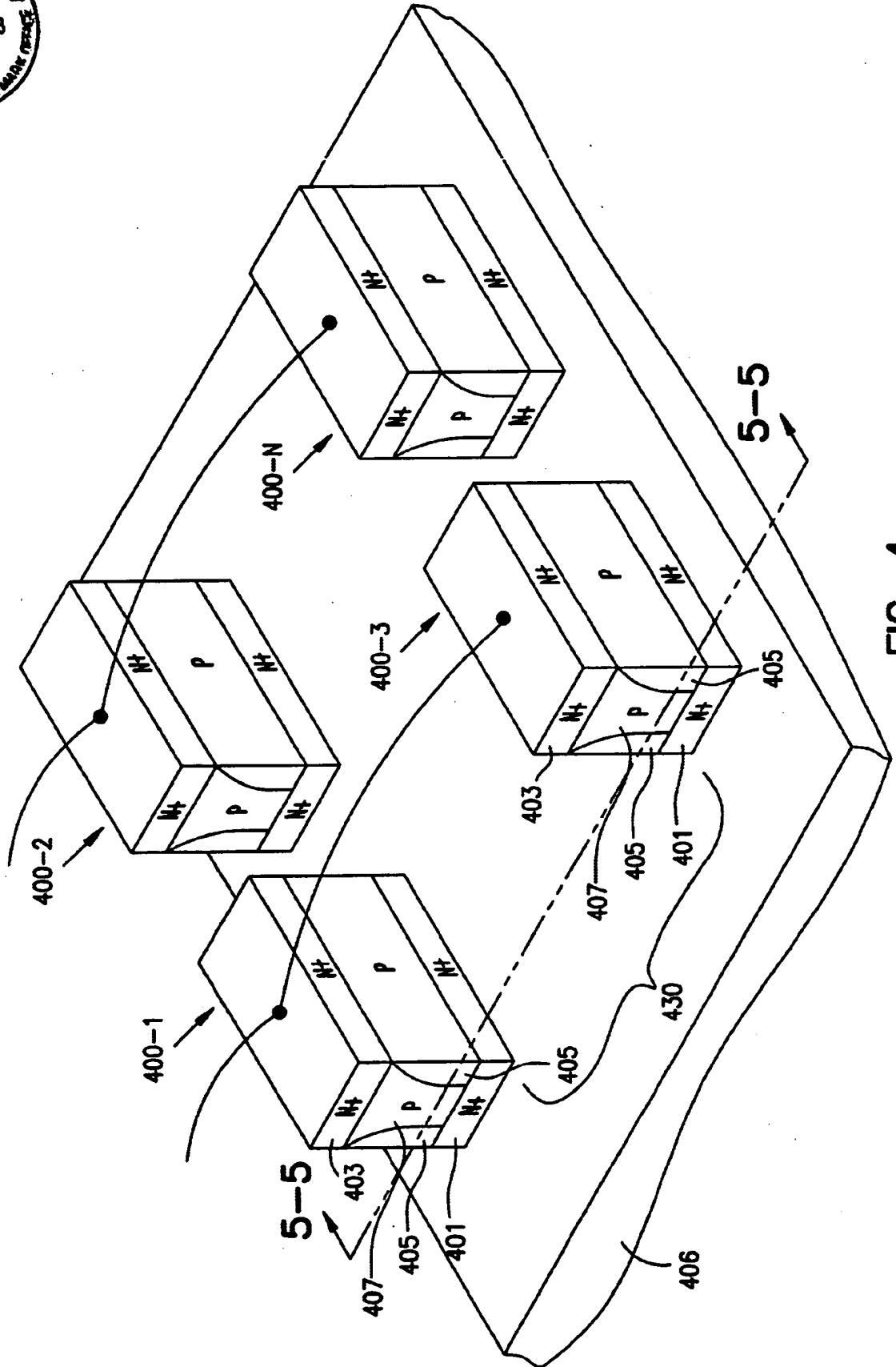


FIG. 4



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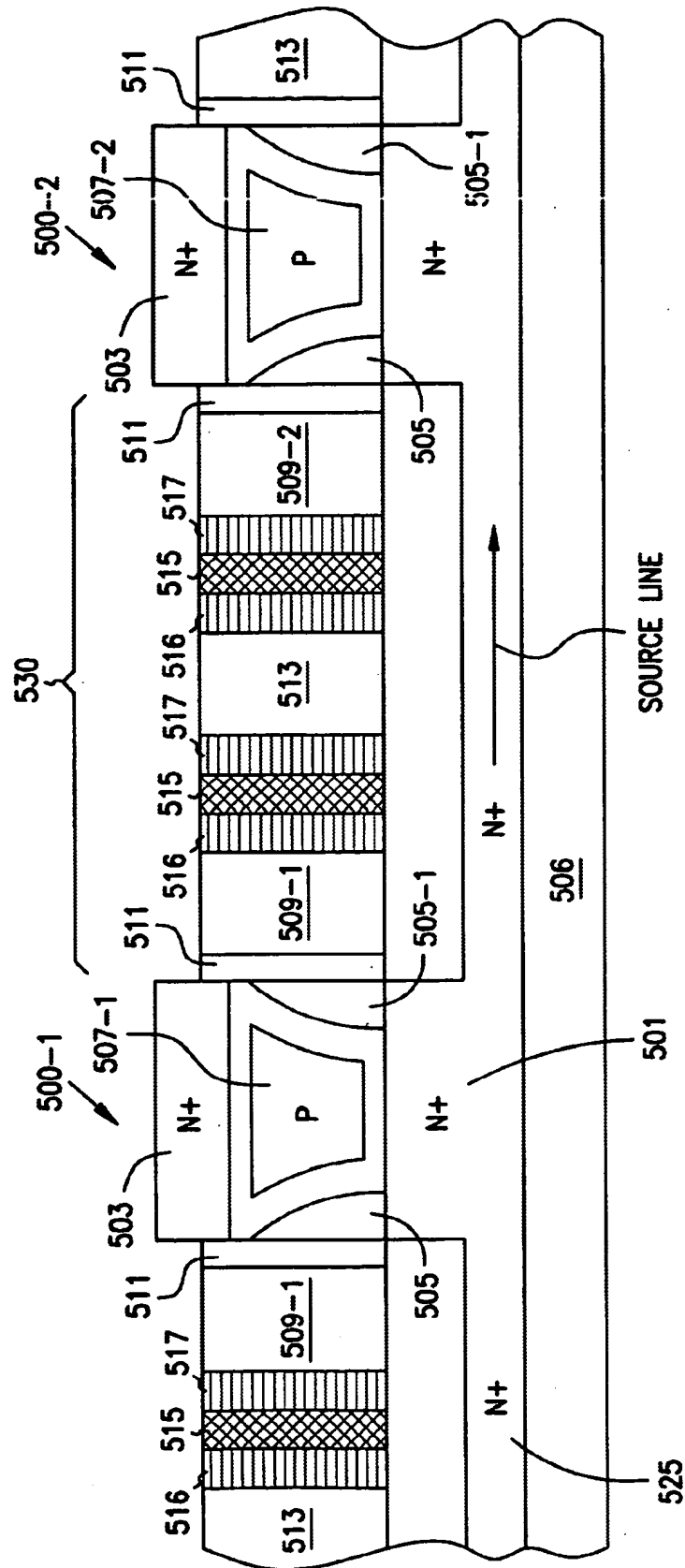


FIG. 5A

A circular stamp from the Intellectual Property Office (IPO). The text "IPO" is at the top, "SEP 22 2013" is in the center, and "PATENT & TRADEMARK OFFICE" is at the bottom.

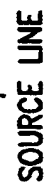


FIG. 5B



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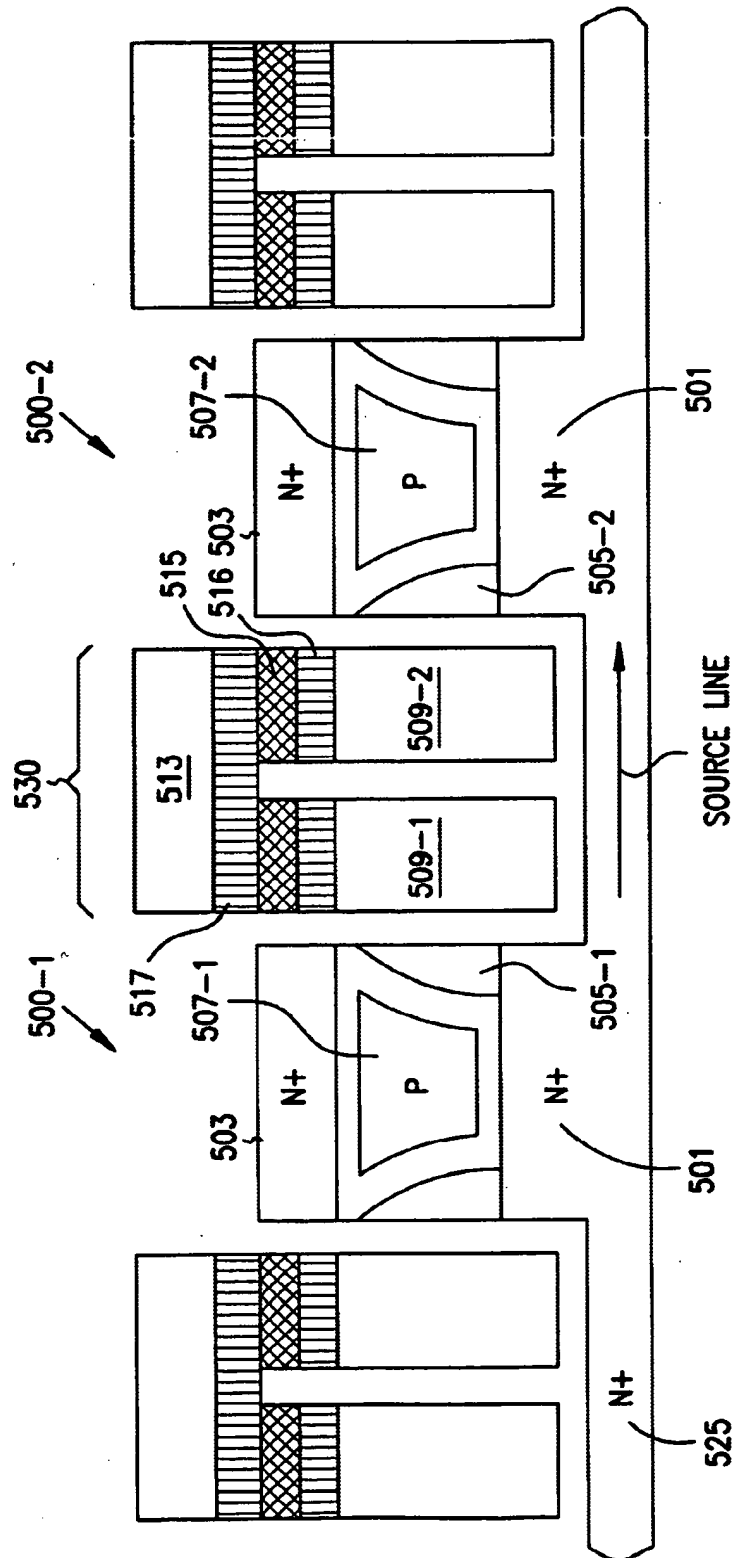
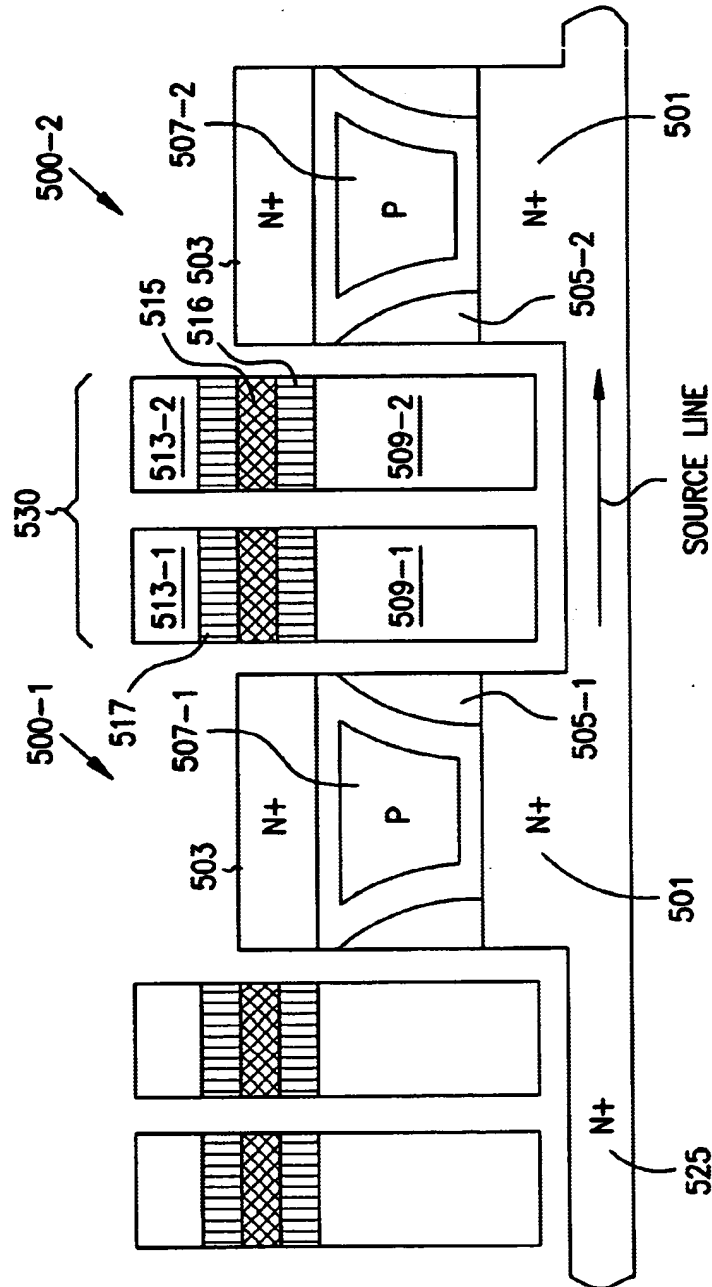


FIG. 5C

FIG. 5D



This diagram shows a cross-sectional view of a semiconductor device. It features two transistors, 500-1 and 500-2, and a source line 501. The transistors are built on a substrate 509. Each transistor has a gate stack 513 on top of a gate oxide 517. The gate stack 513 is composed of a bottom layer 515 and a top layer 516. The transistors are separated by a spacer 503. The source line 501 is a horizontal line at the bottom, with a source contact 525 on the left and a source contact 505-1 on the right. The source line is connected to the source of the transistors. The transistors have a P-type body 507-1 and 507-2, and N+ regions 505-1 and 505-2. The source line is labeled 501 and 525.

FIG. 5E

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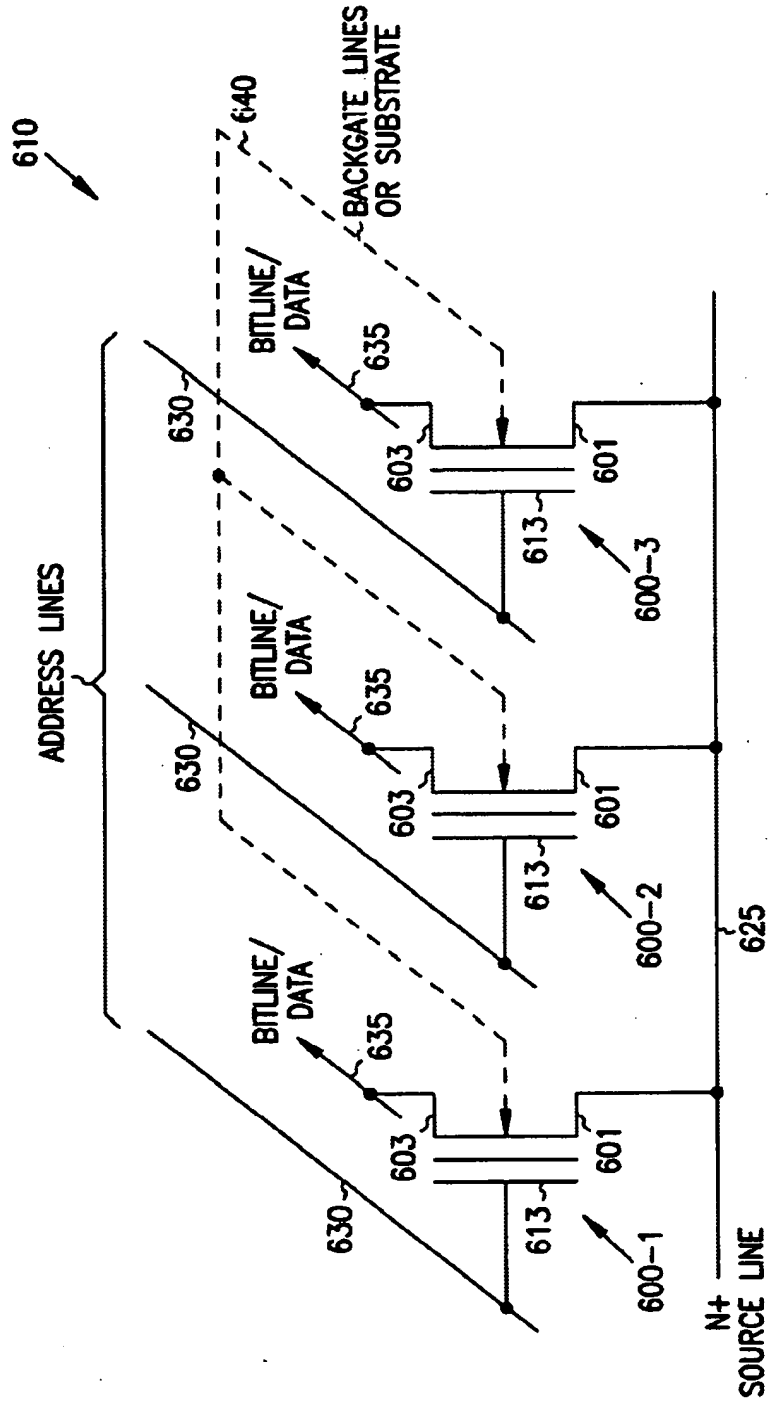


FIG. 6A



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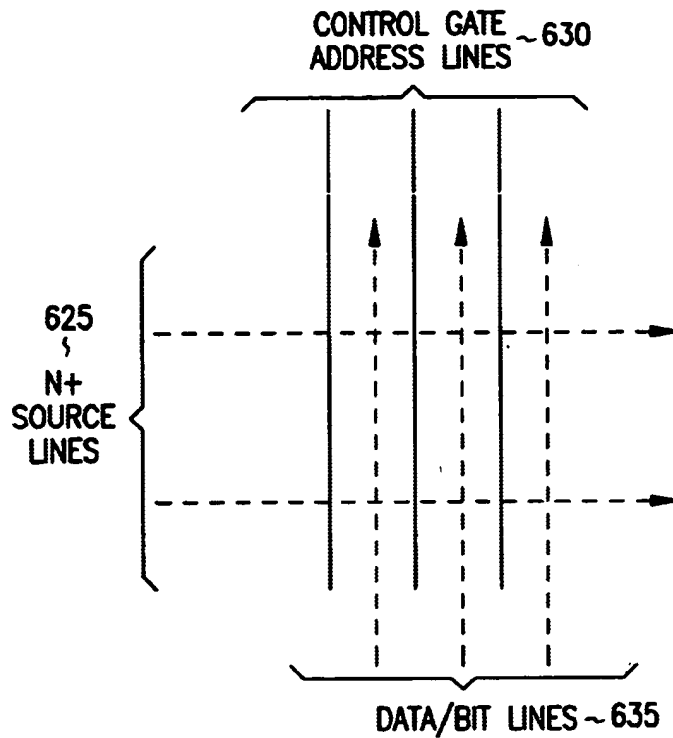


FIG. 6B

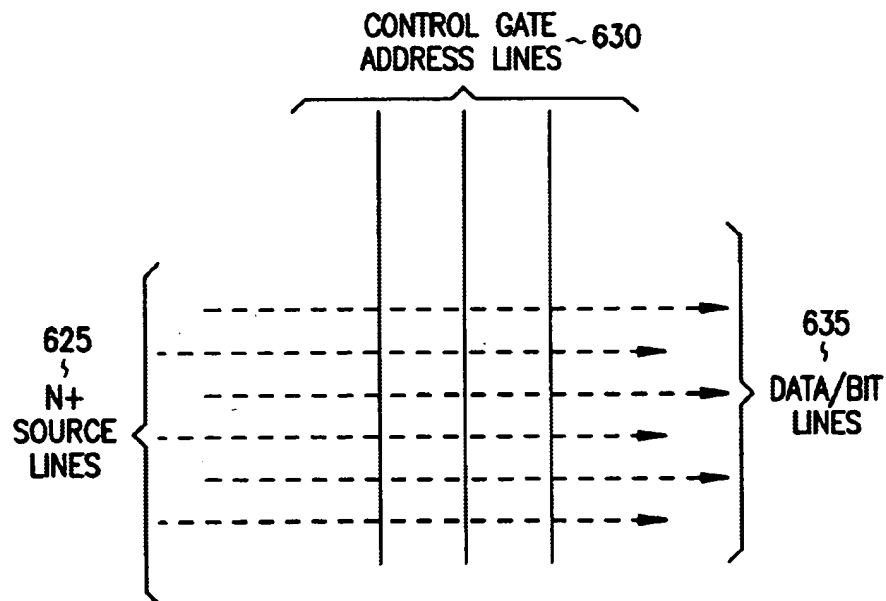


FIG. 6C



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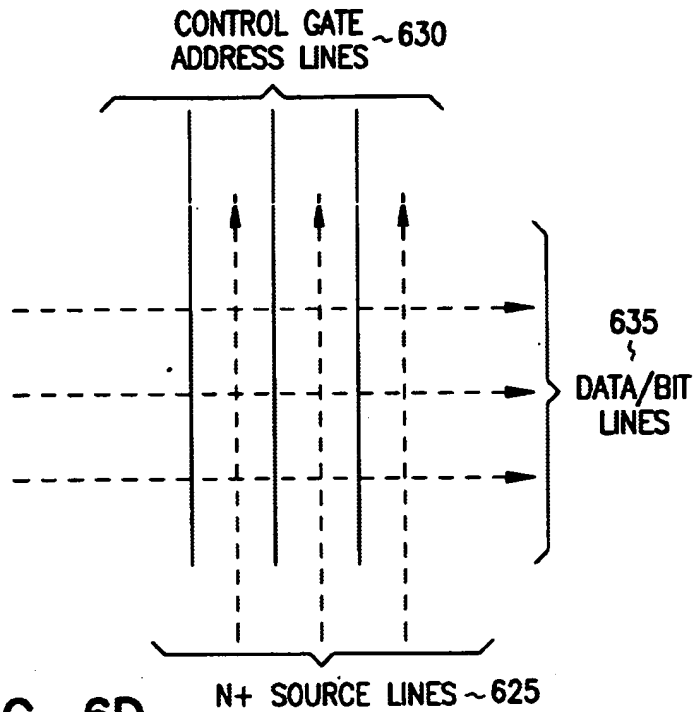


FIG. 6D

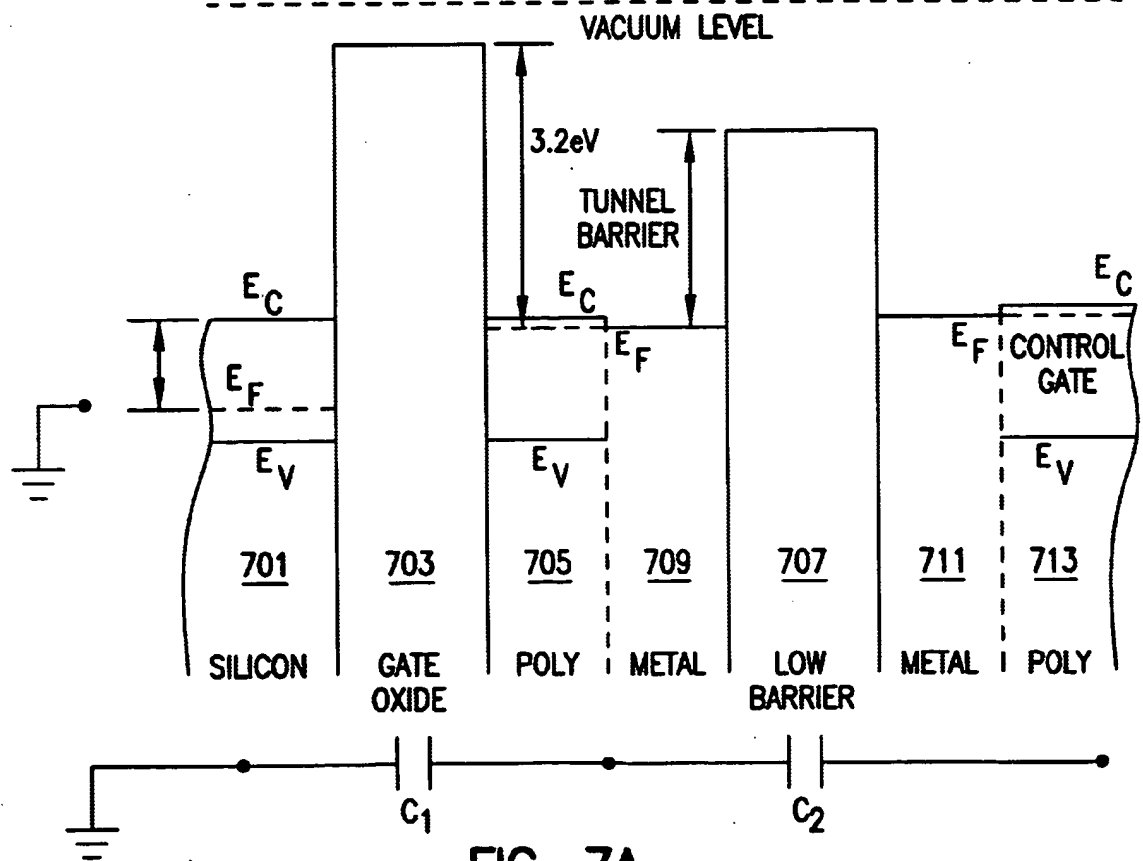


FIG. 7A



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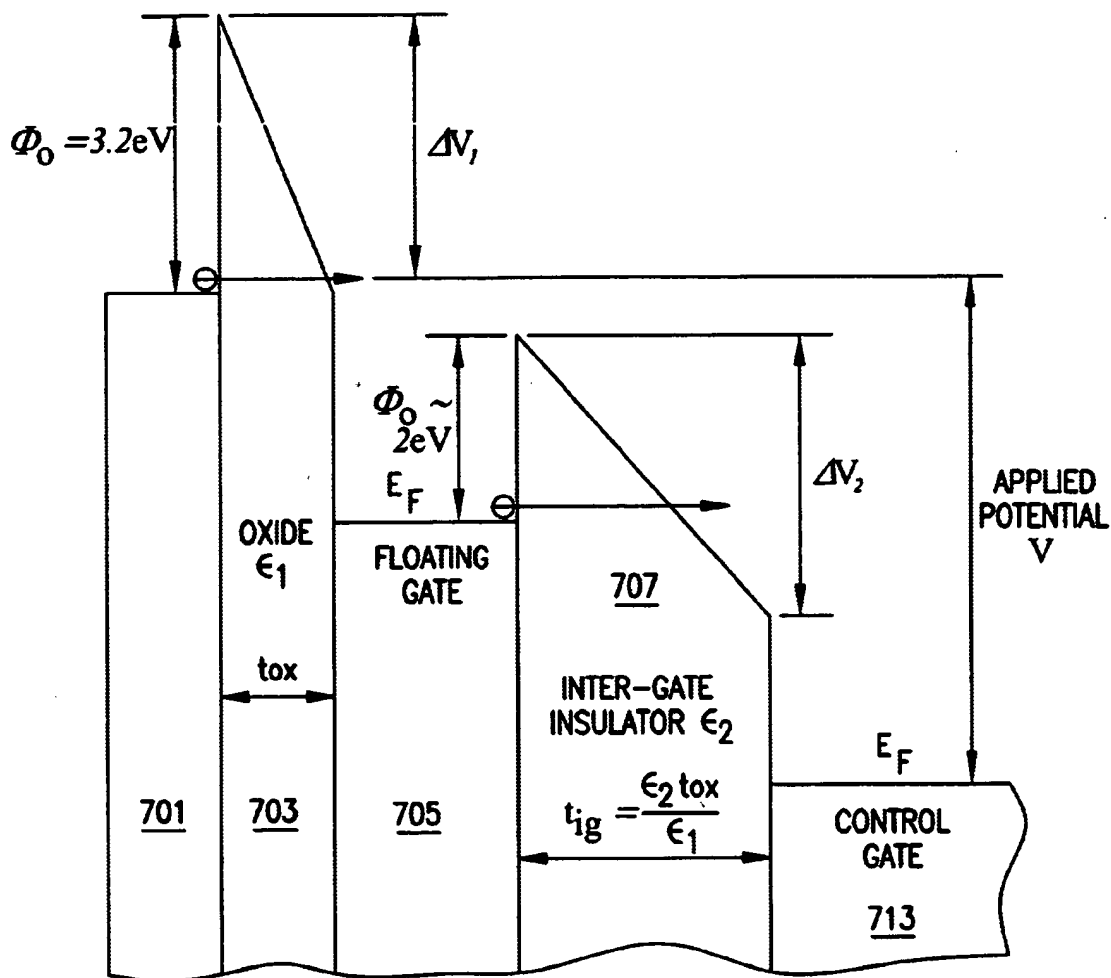


FIG. 7B



TITLE: IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH L
INVENTORS NAME: Leon
DOCKET NO.: 1303.027

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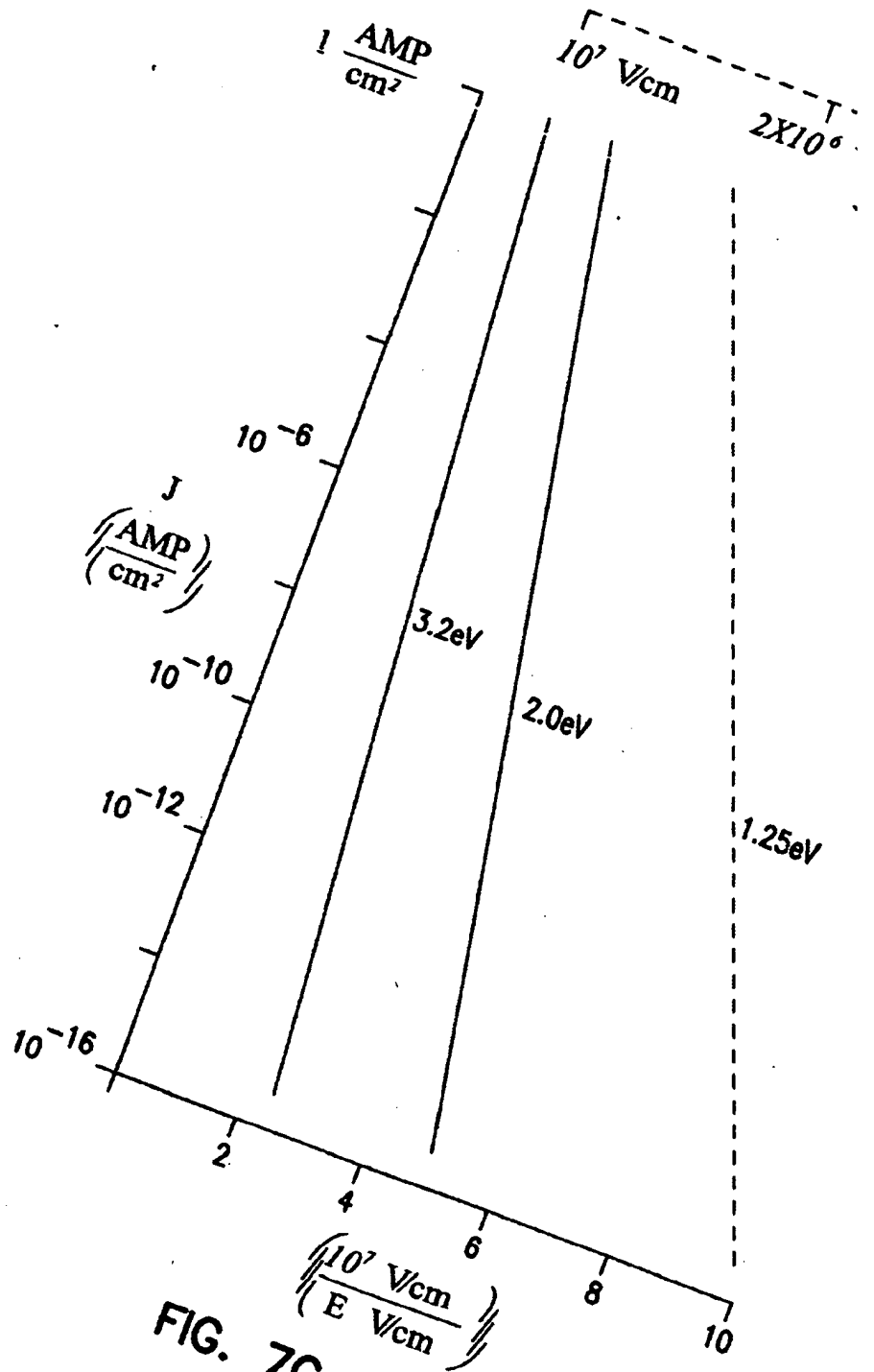


FIG. 7C

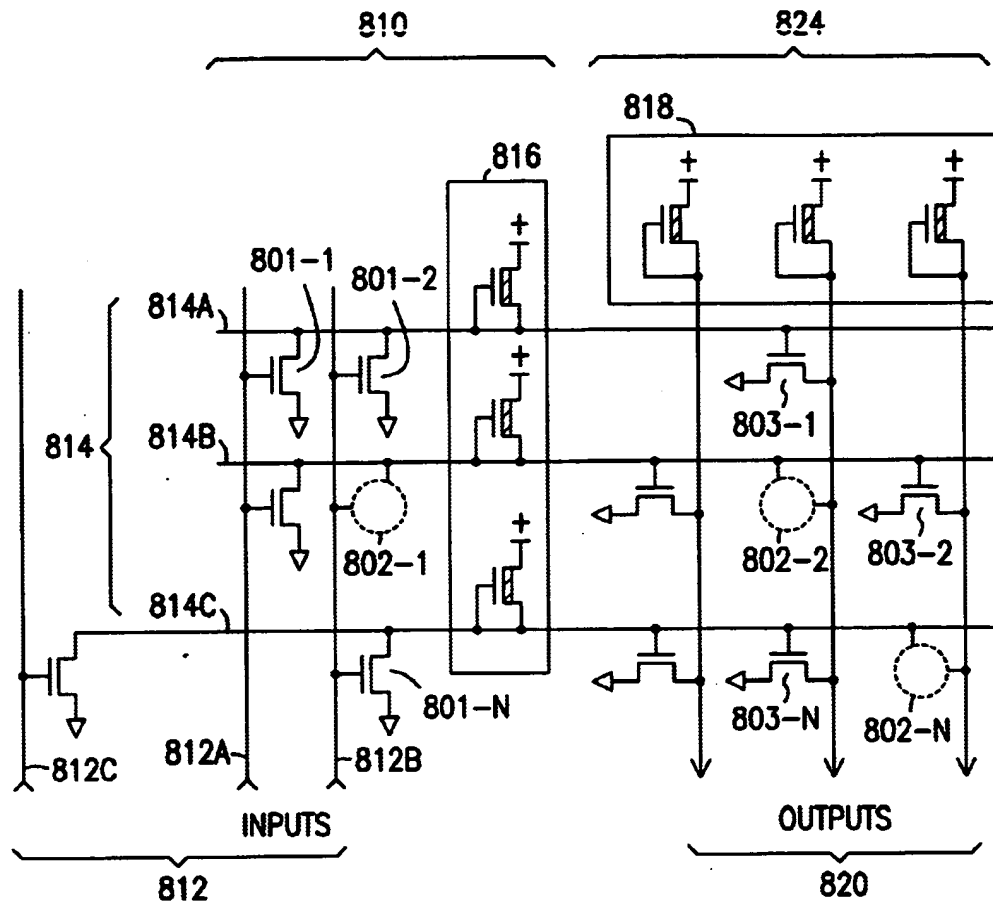
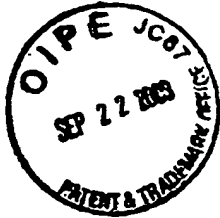


FIG. 8

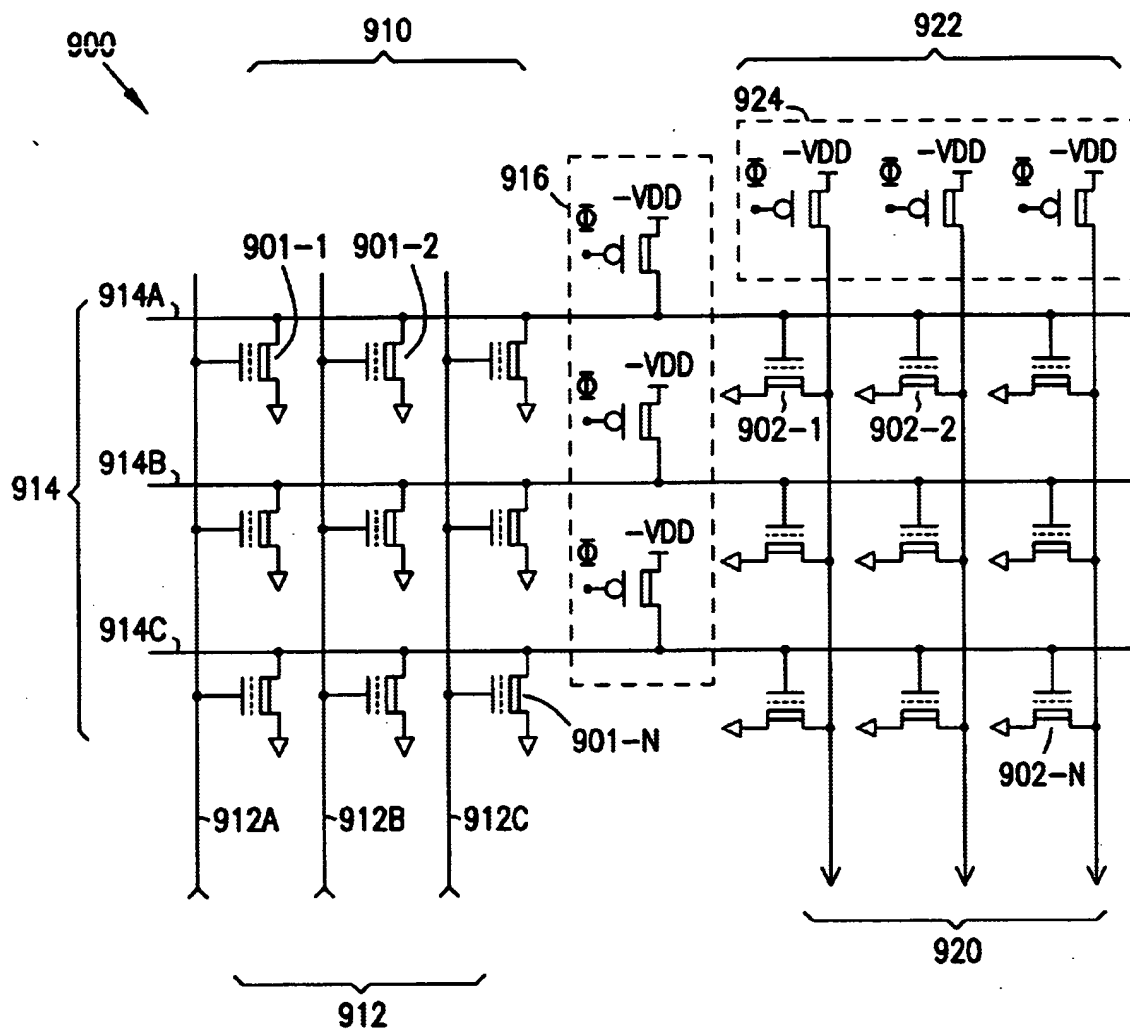
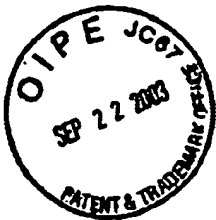


FIG. 9



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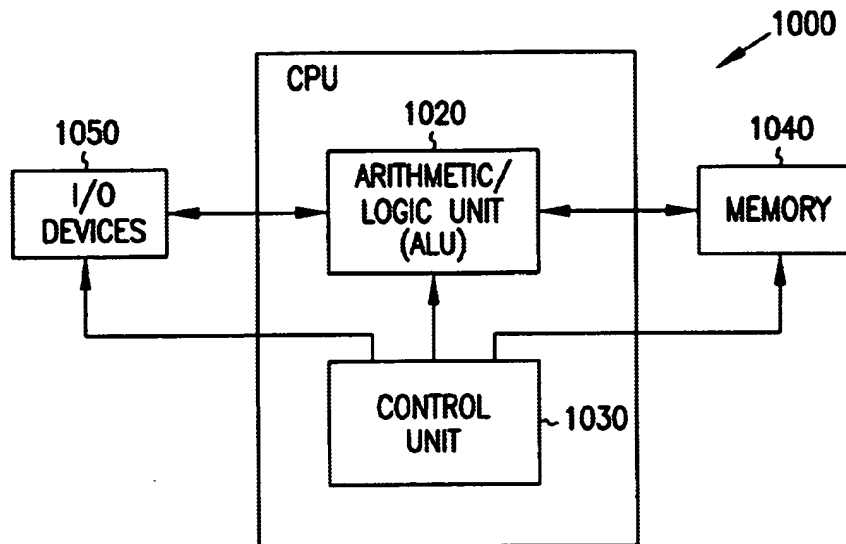


FIG. 10